REMARKS/ARGUMENTS

Reconsideration is respectfully requested.

The Abstract of the Disclosure stands objected to. The replacement Abstract containing all appropriate corrections is attached herewith, and withdrawal of the objection is respectfully requested. A marked-up version showing all changes to the amended Abstract is also attached hereto to aid the Examiner identifying the corrections.

FIGS. 3 and 8 of the drawings stand objected to.

As to FIG. 3, Applicant respectfully note the Specification page 7, lines 15-20, according to which "if the signal **soseb_wt** is in the **high** level, the rising data dinr is transferred to the **odd** global input/output line **giod_od** ... and the falling data dinf is transferred to the even global input/output line giod_ev...." FIG. 3 is consistent with this disclosure where the second pulse of dinr (for example, this could be Q2 of the four data busts Q1-Q2) is transferred to gio_od, because the signal soseb_wt is at the high level. Accordingly, withdrawal of the objection to Claim 3 is respectfully requested.

As to FIG. 8, appropriate corrections have been made to the replacement sheet attached hereto, and withdrawal of the objection is also respectfully requested.

Claims 1-4 are pending in the present application before this amendment. By the present amendment, Claims 1-4 have been amended, and a new Claim 5 has

been added. No new matter has been added.

Claims 1-2 and 4 stand rejected under 35 U.S.C. § 102(a) as being anticipated by the Applicant's admitted prior art (AAPA).

Claim 1, as amended, recites the first and second data buffers that are --controlled **directly** by the **data-in-strobe signal** from the clock pulse generator--. This is one of many distinguishing features of the presently claimed invention. The conventional system as shown in FIG. 1 of the present application processes the first and second data buffers 120, 121 are **not** directly controlled by the data-in-strobe signal from the clock pulse generator 100; rather, they are controlled by, for example, "dinstb_ev" and/or "dinstb_od", which are derived from "dinstb".

Further, Claim 1, as amended, the data are inputted to the claimed "multiplexer" (not directly to the first and second data buffers as in the case of the conventional art as in FIG. 1). The appropriate sequence of data bursts are then outputted from the multiplexer based on the multiplexer control signal (for example, the "soseb_et" signal in FIG. 4) to the first and second data buffers. In contradistinction, in the case of the conventional system of FIG. 1, the data "dinr" and "dinf" are inputted directed to the first and second data buffers 120, 121, and the which data to be outputted to which global line (e.g., "gio_ev" and gio_of") is determined by a the rather complex circuitries including 110, 111 of FIG. 1.

As described in the Specification page 19, lines 1-6, the claimed multiplexer is rather simply constructed when compared to the conventional systems of 110

and 111 of FIG. 1, and this provides substantial advantage to the presently claimed invention by reducing the layout area.

Further, the time for the write operation is reduced according to the presently claimed invention, because the data-in-strobe signal (which may be the write-in-strobe signal that is enabled in the write mode) are applied directly to the data buffers.

At least for the reasons above, the amended Claim 1 and all dependent Claims 2-5 are distinguished from the cited prior art and therefore are in condition for allowance. An indication thereof is respectfully requested.

Claim 3 stands rejected under 35 U.S.C. § 103(a) as being obvious over AAPA.

Applicant respectfully disagrees. According to Claim 3, as amended, the first data buffer (also true for the second data buffer) --has **only one** data input terminal and selectively receives the first data or the second data through the data input terminal controlled **directly** by the data-in-strobe signal--. In contradistinction, the data buffers of the conventional art has more than one data input terminals (e.g., "dinr" and "dinf" terminals of 120 and 121) and are not controlled directly by the data-in-strobe signal. Accordingly, withdrawal of the rejection is respectfully requested.

For the reasons set forth above, Applicant respectfully submits that Claims 1-5, now pending in this application, are in condition for allowance over the cited

references. This amendment is considered to be responsive to all points raised in the Office Action. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the outstanding rejections and earnestly solicits an indication of allowable subject matter. Should the Examiner have any remaining questions or concerns, the Examiner is encouraged to contact the undersigned attorney by telephone to expeditiously resolve such concerns.

Respectfully submitted,

Dated: July 6, 2004

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APPENDIX OF ATTACHMENTS

Application S/N 10/670,613
Reply to Office Action of March 26, 2004

Replacement Sheets of FIG. 8
(a total of 1 sheet of drawing)

and

Annotated Sheets Showing Changes of FIG. 8 in Red
(a total of 1 sheets of drawing)

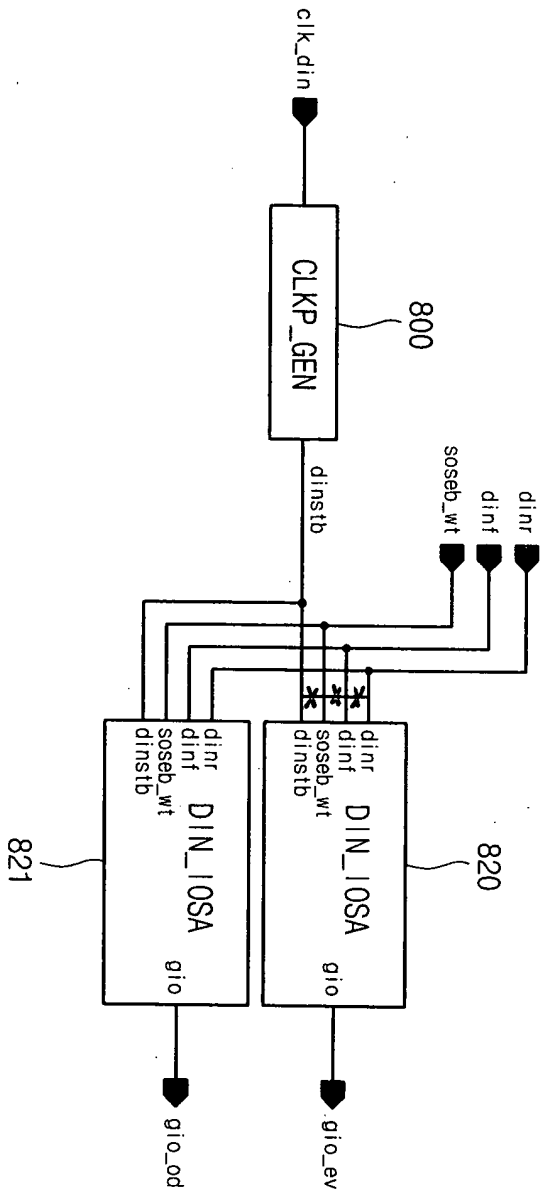
clk_din
CLKP_GEN
800
dinstb
soseb_wt
dinf
dinr
dinr
dinf
soseb_wt
dinstb
DIN_IOSA
gio
820
gio_ev
dinr
dinf
soseb_wt
dinstb
DIN_IOSA
gio
821
gio_od

FIG.8